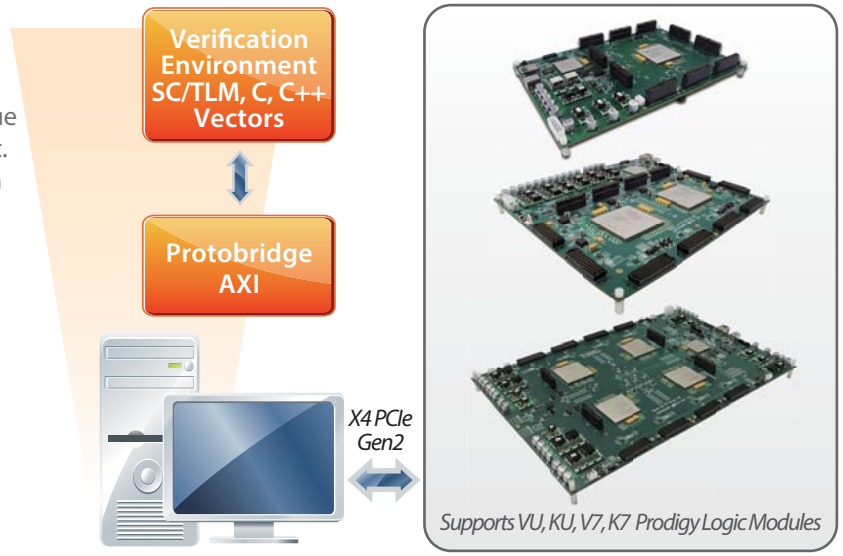
Prodigy™ ProtoBridge™ AXI

An FPGA-Assisted Verification Tool

Overview

FPGA-based prototypes closely resemble final silicon chips in speed and accuracy, providing significant value in full-chip validation and early software development. Realizing these benefits has historically been met with the need to build additional hardware with significant resources and specialized expertise having to be employed to obtain the necessary FPGA connectivity.

The unique Prodigy ProtoBridge AXI FPGA-Assisted Verification Tool uses the widely adopted AXI-4 bus protocol within its patented technology to link the design to the FPGA-based prototyping environment. The result is a high-throughput channel that allows for the transfer of large amounts of transaction-level data between the FPGA(s) and a host computer.



Prodigy™ ProtoBridge AXI hardware setup

Benefits

Technology

Early IP Verification without the complete SoC design

- IP blocks connected to the AXI bus can be verified without processor cores or peripheral blocks
- Early algorithm/architectural exploration can be performed on the FPGA while taking advantage of the FPGA environment's speed performance

Shorten Design Verification Time with a high-throughput channel

- Transaction-level verification is utilized to ensure system-level result accuracy
- C-code is used as a stimulus to reduce the time and effort in creating RTL test benches

Achieve High Product Reliability with improved test coverage

- Create corner test cases in software and run exercises on an FPGA-based prototype
- Run high-performance regression tests on an FPGA-based prototype with vectors stored in host computers

Business

Eliminate Resource & Expertise Constraints by removing the need for the creation of additional specialized hardware and software

Reuse Across Multiple Projects as the flexibility of Prodigy ProtoBridge makes it ideal for any design

Get World-Class Support to help design teams with any issues that arise – something not available with in-house solutions leaving design teams to fend for themselves

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Features

AXI-4 Bus Protocol Between Host PC and FPGA

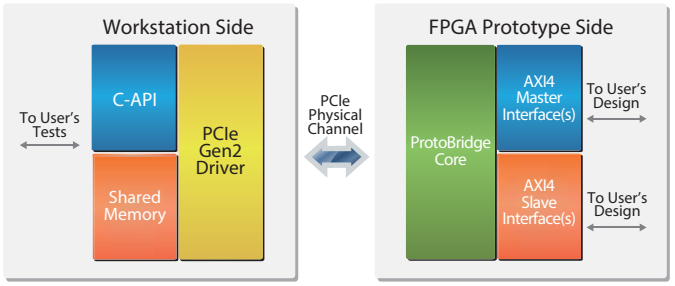
- Instantiation of AXI-4, AXI4-Lite, AXI-3 and AHB bus connections on FPGA ports
- Configurable data width from 32-bit to 1024 –bit
- Support for an independent clock for each Master/Slave instance

Exercise of Large Amounts of Verification Data at High Speed

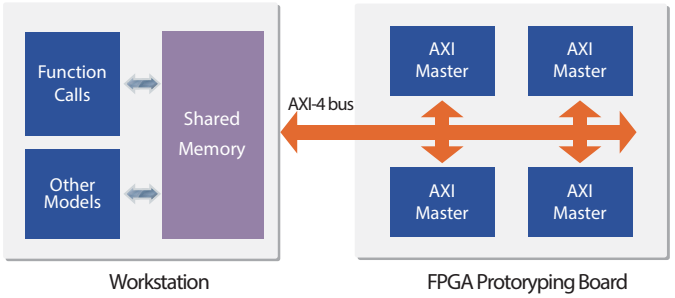
- Transmission through 4-lane PCIe Gen2 between Host PC and FPGA
- Massive data transfer from Host PC to FPGA up to 1000 MB/s
- Support for direct and DMA access modes

Rich Coverage of C Function Calls Between Host PC and FPGA

- System initialization function calls to manage the tool environment
- Interrupt control function calls to identify the source of an interrupt signal for C-API's follow-up actions
- Data read/write function calls to communicate with and operate the FPGA circuit
- DMA transfer function calls to perform DMA operations for large amounts of data



Architecture diagram of ProtoBridge AXI



Logic diagram of Shared Memory

Unique Shared Memory Operation Increases FPGA Prototyping Memory Capacity

- Uses PC memory to store data alleviating the need to store data on the design under test's (DUT's) memory
- Allows DUT to exchange data with host PC's memory
- Simplifies DUT operations of moving the generated data for further design and debug
- Provides easy access to memory content by other tasks running on the host PC at the same time

Compatible with Other ASIC Verification Flows to Expand Usage

- Use with other commercial or in-house verification tools through standard AXI-based C-API

Specifications

FPGA platforms supported

- S2C VU440/KU115 Prodigy Logic Modules
- S2C V7/K7 Prodigy Logic Modules
- User's design can reside on one Prodigy Logic Module or expanded to multiple modules

OSs supported

- Windows 7 (64-bit)
- Ubuntu 14.04.2 (64-bit)
- RHEL 6.5 (64-bit)

PCIe version

- x4 PCIe Gen2

Product Inclusions

- AXI-4 transaction-level interconnection module and Master/Slave interfaces for FPGA integration
- A set of C-API function calls to perform AXI bus transactions in the host computer
- PCIe driver for Linux or Windows operating systems to control Logic Module operations
- C-API reference operations with sample access to FPGA internal memory
- System integration guide to connect user RTL code with the ProtoBridge AXI-4 bus module

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